WHAT IS CLAIMED IS:

1. A method for allocating memory arrangement addresses to a buffer chip, during an initialization mode, for use in addressing one or more memory arrangements connected to the buffer chip, comprising:

receiving first initialization data specifying a first set of available memory arrangement addresses;

associating one or more of the first set of available memory arrangement addresses with the one or more memory arrangements connected to the buffer chip;

generating second initialization data specifying a second set of available memory arrangement addresses comprising the first set of available memory arrangement addresses less the memory arrangement addresses associated with the one or more memory arrangements connected with the buffer chip; and

transmitting the second initialization data from the buffer chip.

2. The method of claim 1, wherein the first initialization data comprise a number of bits, with each bit corresponding to an address for a memory arrangement.

3. The method of claim 1, wherein:

the initialization mode is entered after at least one of: reset or power-up of the buffer chip; and

the initialization mode is terminated after the memory arrangement addresses have been allocated.

4. The method of claim 3, wherein reset or power-up of the buffer chip is followed by an arbitrary memory arrangement address being allocated, so that the command data sent to the arbitrary memory arrangement address is received by the buffer chip .

5. The method of claim 1, wherein the initialization mode is entered in response to command data being received.

6. The method of claim 1, wherein, in a normal mode, the buffer chip receives data and forwards them in parallel to the one or more memory arrangements, receives the data from the one or more memory arrangements and transmits them serially, or both.

7. The method of claim 1, wherein transmitting the second initialization data from the buffer chip comprises transmitting the second initialization data to another buffer chip for use in allocating memory arrangement addresses to memory arrangements connected thereto.

8. The method of claim 7, wherein the buffer chips are connected in series such that a first buffer chip transmits the second initialization data in the form of first initialization data to a second buffer chip.

9. The method of claim 8, wherein the first buffer chip receives the first initialization data from a memory access control unit.

10. The method of claim 8, wherein the second buffer chip transmits the second initialization data to a memory access control unit.

11. A buffer chip for use with one or more memory arrangements, comprising:

a reception unit for receiving first initialization data which specify available memory arrangement addresses;

a transmission unit for transmitting second initialization data; and

an initialization unit for, during an initialization mode, associating memory arrangement addresses with the one or more memory arrangements, the associated memory arrangement addresses being chosen from the available memory arrangement addresses, wherein the initialization unit generates second initialization data specifying the memory arrangement addresses which are still available after the association.

12. The buffer chip of claim 11, further comprising a conversion unit which has a parallelization unit for parallelizing received data and has a serialization unit for serializing data which are to be transmitted.

13. The buffer chip of claim 11, wherein the initialization unit enters the initialization mode after the buffer chip in response to at least one of: reset or power-up of the buffer chip.

14. The buffer chip of claim 11, wherein the initialization unit enters the initialization mode after command data have been received.

15. A memory module comprising:

one or more memory arrangements; and

a buffer chip coupled with one or more memory arrangements, wherein the buffer chip comprises a reception unit for receiving first initialization data which specify available memory arrangement addresses, an initialization unit for, during an initialization mode, associating one or more of the available memory arrangement addresses with the one or more memory arrangements and generating second initialization data specifying the memory arrangement addresses which are still available after the association, and a transmission unit for transmitting the second initialization data.

16. The memory module of claim 15, wherein the memory module is in the form of a DIMM module.

17. A memory system comprising:

a memory access control unit; and

one or more memory modules, each comprising one or more memory arrangements and a buffer chip coupled with one or more memory arrangements, wherein the buffer chip comprises a reception unit for receiving first initialization data which specify available memory arrangement addresses, an initialization unit for, during an initialization mode, associating one or more of the available memory

arrangement addresses with the one or more memory arrangements and generating second initialization data specifying the memory arrangement addresses which are still available after the association, and a transmission unit for transmitting the second initialization data.

18. The memory system of claim 17, wherein a buffer chip of a first one of the memory modules receives first initialization data from the memory access control unit.

19. The memory system of claim 18, wherein a buffer chip of a last one of the memory modules transmits second initialization data to the memory access control unit.

20. The memory system of claim 17, wherein the buffer chips enter the initialization mode in response to at least one of: reset of the memory modules, power-up of the memory modules, and command data.